Set #4

Due Wednesday July 23, 2014

Problems:

1. (Egan 7.2) Given a first-order loop and $K_p = 0.1 \text{ V/rad}$.
   (a) When the reference has a peak deviation of 0.1 rad, what will be the peak deviation of the phase detector output at high modulation frequencies?
   (b) What is the value of $K_v$ for a frequency-demodulation response at $f_m = 1 \text{ kHz}$ that is 6 dB below the DC response.
   (c) If $K_v = 1 \text{ kHz/V}$, at what modulation frequency will the phase demodulation output be 20 dB below its high frequency value?
   (d) What peak voltage injected after the phase detector will produce 0.01 rad peak phase deviation at low frequencies?

2. (Egan 7.5) A loop has an integrator-and-lead filter with unity open-loop gain (straight-line gain approximation) at 10 kHz and a zero at 5 kHz. What is the peak phase error when the input reference signal is frequency modulated at a peak deviation $\Delta f = 4 \text{ kHz}$? At what frequency $f_m$ does it occur?

3. (30 bonus points) A phase-locked synthesizer is designed to have output frequency $f_{\text{out}} = 1.578 \text{ GHz}$ using a reference frequency of 2 MHz. The design uses a charge-pump PLL similar to Set 2 problem 5a. The baseband PLL model is shown below (see Hanumolu¹ and/or solutions to Set #2 problem 5a).

![ PLL Diagram ]

3. (cont.) The phase detector is modeled as being linear over the required lock range, but there
is also a ripple or leakage component summed in at the reference frequency

\[ i_d(t) = \left[ \theta(t) - \dot{\theta}(t) \right] \frac{I_{cp}}{2\pi} + A_r \cos(2\pi f_{ref} t) \]

(a) Choose \( K_{LF} \) for a phase margin, \( \phi_m \), of 70°. The cross-over frequency, \( f_c \), should be at about 200 KHz.

(b) Using a narrowband FM approximation for sideband generation, find the maximum value for \( A_r \) in the ripple model, so that the spur level on the VCO output is at least -60 dBc.

(c) Plot the frequency switching transient if \( N \) is programmed to step the output frequency from 1.200 GHz to 1.578 GHz.

4. (Egan 8.1 modified) A loop has a double-balanced mixer phase detector with a (maximum) gain of \( K_p = 0.1 \text{ V/cycle} \). The tuning characteristic of the oscillator has a 40-MHz/V slope. The loop filter is shown below. The VCO is 90° out of phase with an input signal to which it is locked when the frequency is 30 MHz (note this is a locked 0° phase error condition).

\[
\begin{array}{c}
\text{10 kΩ} \\
\downarrow \\
50 \text{Ω} \\
\downarrow \\
1 \text{μf}
\end{array}
\]

(a) If the input frequency drifts, how high can it go before the loop will lose lock? Give frequencies in Hz.

(b) After lock is broken, the input frequency is lowered again. At what frequency can lock be reacquired? What are the restrictions on the formula that you used and how well are they met (give numerical values)?

(c) At what difference between input frequency and VCO center frequency \( f_c \) will cycle skipping stop? What are the restrictions on the formula that you used and how well are they met (give numerical values)?

(d) How long will it take to stop cycle skipping if the input signal is 14 kHz above \( f_c \)? What are the restrictions on the formula that you used and how well are they met (give numerical values)?