Set #2

Due Friday September 29, 2017

Problems:

1. We have a phase detector with sensitivity $K_p = 1$ v/rad and VCO modulation sensitivity of $K_v = 1$ MHz/v. The phase detector has a spurious time constant $\tau_p = 31.8$ ns (-3 dB cutoff frequency of $f_c = 5$ MHz) and the VCO has a spurious time constant $\tau_v = 1.59 \mu$s (-3 dB cutoff frequency of $f_c = 100$ kHz. Assume $N = 1$.

   (a) Suppose we wish to construct an approximately first-order loop, i.e., $F(s) = 1$, then what constraints must be imposed on $K_{LP}$ to insure a phase margin of at least $45^\circ$. Is this reasonable?

   (b) Construct an approximately second-order loop using

   $$F(s) = \frac{1 + s\tau_2}{s\tau_1}$$

   Choose $\omega_n = 1000$ rad/s and $\zeta = 1$. Find $\tau_1$ and $\tau_2$, and the approximate phase margin, $\phi_m$, using straight line Bode analysis. You may use Python or MATLAB if you wish to get a more exact phase margin.

2. The charge-pump PLL has a digital phase detector which typically produces current pulses in response to a phase/frequency error between the inputs to the phase detector. For now we simply assume that in the linear model, the phase error, denoted $i_d(t)$ in the figure below, has gain $K_p$ A/rad. The loop filter is a transimpedance circuit, that is it converts an input current to an output voltage. A pure gain, denoted $K_{LF}$, may also be part of the loop filter. As usual the VCO has gain $K_v$ MHz/v and a frequency divide by $N$ is likely here as well. The circuit shown below results in either a type II third-order or 4th-order PLL. In practice this configuration is popular in synthesizers and ASIC clock generation subsystems.

![Charge Pump PLL Diagram](image)
2. (continued)
   (a) Find the loop filter \( s \)-domain transfer function in terms of \( C_1, C_2, \) and \( R_1 \) (the optional lowpass section omitted). Verify that the closed-loop transfer function, \( H_3(s) \) is a 3rd-order type 2 loop. Find an expression for the phase margin.
   (b) Find the loop filter \( s \)-domain transfer function in terms of \( C_1, C_2, C_3, R_1 \) and \( R_2 \), including the optional lowpass section. Verify that the closed-loop transfer function, \( H_4(s) \) is now a 4th-order type 2 loop. Find an expression for the phase margin.

3. (Egan 6.4) A PLL has a passive lead-lag loop filter as shown below

\[
\begin{array}{c}
\text{in} \quad u_1(t) \\
\overline{R_1} \\
\overline{R_2} \\
\overline{C} \\
\text{out} \quad u_2(t)
\end{array}
\]

with \( R_1 = 3 \) k\( \Omega \), \( R_2 = 1 \) k\( \Omega \), and \( C = 0.16 \) \( \mu \)F. \( K_p = 0.5 \) V/rad and \( K_v = 10,000 \) (rad/sec)/V. What is the phase error in the locked loop 160 \( \mu \)s after a 0.2 radian input phase step? Show your work.

4. A particular third-order PLL has the following loop filter
   \[ F(s) = 1 + \frac{a}{s} + \frac{b}{s^2} \]
   (a) Construct the Routh array and determine the conditions on absolute BIBO stability.
   (b) For \( a = 10 \) and \( b = 5 \) find the value of loop gain \( K \) for which a pair of poles of the closed-loop system lie on the \( j\omega \) axis. What are the pole locations. The Python control package function \( \text{rlocus}(\text{sys},K) \) should be useful here.

5. Using the loop filter of problem 4, suppose the input phase deviation is of the form:
   \[ \theta(t) = \left[ \theta_0 + \Omega_0 t + \frac{1}{2} \Lambda_0 t^2 + \frac{1}{6} \Gamma_0 t^3 \right] u(t) \]
   (a) Find the steady-state phase error \( \phi_\infty \) in terms of the input parameters.
   (b) With \( \theta_0 = 10^\circ, \Omega_0 = 2\pi \times 500 \) rad/s, \( \Lambda_0 = 2\pi \times 50 \) rad/s\(^2\), and \( \Gamma_0 = 2\pi \times 5 \) rad/s\(^3\), find the loop gain \( K \) such that \( \phi_\infty = 1^\circ \) when \( a = K/2 \) and \( b = K/4 \).
   (c) Construct a nonlinear simulation model for this loop using the techniques described in class, that is extending \texttt{synchonization.PLL1}. Apply the loop dynamics of part (b) to study the complete transient response. Check to see that the steady-state phase error is indeed 1\( ^\circ \). Assume a sinusoidal phase detector. Note that the analysis of (b) assumes a linear loop. If you have problems with the nonlinear simulation you might at first test with the linear model. Choose \( f_s = 1000 \) Hz for the sampling rate.
(d) Using the simulation model of (c) apply just a frequency ramp, \( \Lambda_0 \). Through experimentation find the value of \( \Lambda_0 \) where the loop begins to slip cycles. Since this is a type 3 loop, what should \( \phi_{ss} \) always be?