1 Introduction

The purpose of this laboratory exercise is to design, build, and experimentally characterize a second order phase-lock loop (PLL). Two types of loop filters will be investigated, the lead-lag filter and the integrator with lead compensation. The PLL will be designed to operate at a specific carrier center frequency, $f_0$, loop natural frequency, $\omega_n$, damping factor, $\zeta$, and hold-in range, $\Delta f_H$. Note that the hold-in range is the maximum amount the input frequency can deviate from the quiescent VCO frequency and have the loop remain in lock. This term assumes the PLL is initially in a locked state.

The PLL will be constructed using for the most part pre-assembled circuit function blocks mounted on an RF bread-board. The loop filter will use a bi-fet op-amp with appropriate resistor and capacitor elements determined from the design equations. Before the actual PLL design begins, the phase detector and the VCO must be characterized. For this experiment the phase detector is a surface mount packaged double-balanced mixer using transformers and a diode ring (Mini-Circuits ADEX-10L) and the VCO is a surface mount packaged part (Mini-Circuits JTOS-75). The VCO output is buffered through a surface mount two-way 50 ohm power splitter (Mini-Circuits ADP-2-1W) so that a 50 ohm test port is always available to drive a spectrum analyzer/scope/frequency counter. The reference signal $s(t)$ will be obtained from an 80 MHz Function/Arbitrary Waveform Generator, (Agilent 33250A).

The system requirements are to design a second order PLL to initially have:

- Nominal carrier center frequency $f_0 = 50.000$ MHz
- Loop Hold-In Range $\Delta f_H = 5$ MHz
- Natural Frequency $\omega_n = 5 \times 10^4$ rad/sec
- Damping Factor $\zeta = 1/\sqrt{2}$

Later in the experiment you may want to change some of these specifications, if time permits.

The loop filters considered will be a lead-lag filter with finite DC gain and an integrator with lead correction filter having in theory infinite DC gain. The close-loop parameters $\omega_n$ and $\zeta$ will be experimentally measured, and step response measurements will be taken.

If time permits simple nonlinear acquisition measurements will be taken. Additionally, the phase noise will also be measured and compared with a behavioral level model implemented using Spice.

1.1 Schedule

Laboratory teams will be limited to at most two members. I encourage you to work together, hence do not work alone unless you feel this is your only option. The class meeting of Monday October 16 will be the first formal class meeting time assigned to work on this lab experiment. We will
continue work on the experiment the following Monday. You may need to finish up work on the experiment during other times you and your partner choose.

I expect a formal lab report to be written, which documents the results of this experiment. One report per team. The report is due no later than Friday November 13, 2017.

2 PLL Subsystem Characterization

For the design of a PLL from scratch you would first consider the system requirements before selecting any of the loop subsystems (i.e. phase detector, loop amplifier/filter, and VCO). For this experiment you do not have this kind of freedom. The laboratory has been designed to work with the available equipment, with certain compromises being made. A block diagram of the PLL showing the various laboratory subsystems is given in Figure 1. Everything to build the complete PLL, except the Agilent 33250A reference source, is mounted on the test board. A ±12v power supply is also needed to power the active circuits on the board. The VCO needs 12v and the op-amp requires ±12v. A corresponding photograph of just the PLL module itself is shown in Figure 2.

![Figure 1: Laboratory PLL block diagram.](image)

The relevant elements are noted in this photo. Additional circuitry on the board not immediately evident from the block diagram and photo are an RC lowpass filter consisting of a 51 ohm resistor and a 0.01 μf chip capacitor, and power decoupling filters on the input power jacks to the board and additionally on the VCO input power pin. These two circuits are detailed in Figure 3 One other circuit item mounted on the board next to the op-amp is a 5 kΩ multi-turn potentiometer. This will be used to form an adjustable bias voltage which can be used create a level-shifter for setting the VCO quiescent frequency to 50 MHz.

To reduce Figure 1 to the equivalent linear PLL block diagram we first must characterize the Mini-Circuits JTOS-75 VCO to obtain $K_v$, and then characterize the phase detector to obtain $K_p$. 
Figure 2: PLL module photograph.

Figure 3: Details on phase detector lowpass and power supply decoupling circuits.
2.1 Laboratory Exercises

2.1.1 VCO Characterization

Detailed JTOS-75 VCO data sheets can be found in the appendix. We wish to characterize the VCO in the vicinity of 50 MHz to determine an approximate value for $K_v$. The VCO out port on the board can be used to drive a frequency counter. This port is the result of feeding the VCO output through a 2-way equal gain, equal phase, power splitter (Mini-Circuits ADP-2-1W).

From the data sheet the VCO produces 50 MHz when the tuning voltage is at about 7 v. To actually move the VCO frequency you will need to connect a bias supply to the VCO control input. This can be supplied from an additional supply or by configuring an op-amp as a level-shifter and using the multi-turn pot already on the board. A possible configuration for an op-amp level-shifter bias supply circuit is shown in Figure 4.

![Figure 4: A detailed look at the op-amp physical configuration in the PLL module.](image)

- Obtain frequency as a function of control voltage data so you can plot $f_0$ versus voltage from 40 to 60 MHz. This will not be a perfectly straight line. The slope at 50 MHz however is a good estimate for $K_v$. Remember later during loop calculations to convert $K_v$ to rad/s/v.

- A second plot to make from the recorded data is a plot of $K_v$ in MHz/v as a function of center frequency. A plot similar to this is in the data sheet, so you have something to compare to for your particular VCO.

The fact that VCO sensitivity is not constant gives you some idea of how loop parameters will change should you want to move the center frequency of the loop. For future reference, note that the VCO data sheet indicates that the modulation bandwidth of the VCO is 125 kHz, this is related to the VCO spurious time constant.
2.1.2 Phase Detector Characterization

The phase detector consists of a Mini-Circuits ADEX-10L double-balanced mixer (DBM), followed by a lowpass filter to remove the double frequency terms. Note that in the analysis of the complete PLL this lowpass filter constitutes a spurious time constant. Since the mixer output impedance is approximately 50 ohms, the R value in the lowpass filter is actually about 100 ohms. The specifications for the ADEX-10L mixer can be found in the Appendix.

A DBM phase detector is very similar to an ideal multiplier or sinusoidal phase detector. The phase detector constant $K_p$ is a function of the signal amplitudes at both the RF (reference source) port and the LO (VCO) port. For this experiment the RF drive level will be -5dBm. The Agilent 33250A, which serves as the reference signal source, can be easily configured to this output power level via front panel settings.

To experimentally determine $K_p$ use the test set-up shown in Figure 5. Two sinusoidal signals, each at approximately 50 MHz, are input to the DBM RF and LO ports. The input signals are of the form

$$v_{RF}(t) = A \sin(2\pi f_0 t + \theta)$$
$$v_{LO}(t) = B \cos(2\pi f_0 t + 2\pi \Delta f t + \hat{\theta})$$ (2)

where $\Delta f$ is a small frequency difference between the two signals. Using a sinusoidal phase detector model the phase detector output, assuming the RC lowpass filter removes the double frequency term is

$$v(t) = \frac{AB}{2} K_m \sin(2\pi \Delta f t + \theta - \hat{\theta})$$
$$= K_p \sin(2\pi \Delta f t + \theta - \hat{\theta})$$ (3)

where $K_m$ is the mixer multiplication constant and

$$K_p \equiv \frac{AB}{2} K_m \text{ v/\text{rad}}$$ (4)

![Figure 5: Test set-up for measuring phase detector gain.](image-url)
is defined to be the phase detector gain. From (3) it follows that \( K_p \) can be experimentally determined by observing the phase detector output for small \( \Delta f \). Note that if \( \Delta f \) is not small, then the phase detector lowpass filter will also significantly attenuate the frequency difference term as given by (3). When the phase detector is placed in the PLL and the loop is locked, then of course \( \Delta f \) is essentially zero.

For proper operation of a DBM the LO drive level is typically at least 10 dB higher than the RF power level. For the ADEX-10L the recommended LO drive level is 4 dBm to insure minimal conversion loss (see the mixer specs in the appendix). The VCO output is nominally +8 dBm, but the 2-way splitter drops 3 dB, so the LO input to the mixer should be about +5 dBm. It is important to note here that for the 3 dB splitter loss to hold, the VCO test port must be kept terminated into a 50 ohm load, i.e., some test instrument or if need be a 50 ohm BNC terminator, which can be found in the lab. An RF level of -5 dBm is 10 dB below the LO level, and according to the data sheet the conversion loss at 50 MHz should be about 7.2 dB (ideally 6 dB due to the 1/2 factor of the trig identity of (3)).

- Using the test set-up of Figure 5 apply 50 MHz sinusoids to both the RF and LO ports of the ADEX-10L mixer (phase detector). The LO power level is fixed at about +5 dBm assuming the VCO test port is properly terminated. Verify the VCO test port power using the spectrum analyzer to so you know approximately what the true LO drive level really is.

- Take measurements to determine \( K_p \) with the RF level at -15, -10, and -5 dBm. Comment on the linearity of \( K_p \) in response to changes in the RF power level. You will need to make \( \Delta f \) as small as possible to insure that the lowpass filter does not introduce error into your measurement. The waveform that you see on the oscilloscope will look like a frequency modulated sinewave. By increasing \( \Delta f \) you will see the envelope of the output signal shrink due to the lowpass filtering action.

It will be hard to make the difference frequency to stand still, since the VCO wants to drift when in an open-loop configuration. Just changing the VCO test port load termination will cause some frequency pulling.

### 3 Second Order PLL with Lead-Lag Loop Filter

Now that the phase detector and VCO gains have been determined, the design of the loop filter may proceed. In this section of the experiment an active lead-lag loop filter with transfer function

\[
F(s) = \frac{1 + s\tau_2}{1 + s\tau_1}
\]

will be implemented using the op-amp circuit shown in Figure 6. Since the VCO must be biased to the specified 50 MHz center frequency, it is convenient to incorporate a level-shifter into the loop filter. One possible configuration is shown in Figure 7.
3  SECOND ORDER PLL WITH LEAD-LAG LOOP FILTER

Figure 6: Basic lead-lag active loop filter.

Figure 7: Lead-lag active loop filter including a level shifter for VCO center frequency bias.
3.1 Laboratory Exercises

The loop filter components $R_1$, $R_2$, $R_3$, and $C$ must be determined such that the system requirements are satisfied. Designing for a specific natural frequency, $\omega_n$, and damping factor, $\zeta$, follows directly from the PLL linear model equations. The loop hold-in range can be determined from the phase detector characteristic and the dc loop gain. Since the phase detector has a maximum output of $K_p \sin(\pi/2) = K_p$, the hold-in range of the PLL is equal to the dc loop gain $\pm K_p F(0) K_v = \pm K F(0)$ rad/sec. This is the maximum offset frequency that the VCO can be tuned to, with respect to the VCO quiescent frequency, and still remain locked. Note that the loop filter of Figure 6 has a dc gain magnitude of $R_2/R_1$.

- Comment on the significance with respect to second order PLL design, of the spurious constant due to the lowpass filter in the phase detector and spurious time constant of the VCO.

- Determine suitable component values for $R_1$, $R_2$, $R_3$, and $C$ with an RF power level of -10 dBm to achieve $\omega_n = 5 \times 10^4$ rad/s, $\zeta = 1/\sqrt{2}$, and $\Delta f_H = \pm 5$ MHz. Since a wide range of capacitor values is not available in the lab, it is suggested that you initially choose a convenient value for $C$.

- Construct the loop filter using an TLO-82 (LF353), or similar 8-pin DIP dual op-amp as found on the experiment module. A description of the TLO-82 and its pin-out are given in Figure 8. More detailed TLO-82 specifications can be found in the appendix.

- Place the loop filter into the PLL as shown in Figure 1. Initially you may want to leave the connection from the phase detector output to the loop filter input open. Do connect the loop filter with level-shifter output up to the VCO input. This will allow you to adjust the VCO quiescent to approximately 50 MHz before closing the loop. When the loop is closed, the quiescent frequency will shift slightly due to a small offset voltage in the mixer (phase detector) output.

- Now close the loop by connecting the phase detector output to the loop filter input. Verify phase lock by observing the VCO output on the Agilent 4395A spectrum/vector network analyzer, or HP 4195A spectrum/vector network analyzer. The spectrum analyzer can be directly connected to the VCO output using the RF power divider output port supplied on the experiment module. You may have to adjust the level shifter offset slightly to bring the loop into lock. When in lock discrete frequency sidebands present on the VCO output should disappear.

- Experimentally determine the loop hold-in range, $\pm \Delta f_H$, by slowly adjusting the frequency of the input signal (RF port) above and below 50 MHz (the loop must be locked to begin with). Record the upper and lower frequencies, if possible using a frequency counter, where the PLL just breaks lock. The difference between these upper and lower lock frequencies is by definition twice the hold-in range, $\Delta f_H$.

- Experimentally determine the pull-in range, $\Delta f_p$, by increasing/decreasing the input frequency until the loop breaks lock. Then slowly move the input frequency in the other direction until the loop just pulls in. When done from both directions you will be able to determine $2\Delta f_p$, and hence $f_p$. You should find that $\Delta f_p < \Delta f_H$. 

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.
The next exercise will be to experimentally determine the second order loop parameters $\omega_n$ and $\zeta$. The test set-up is shown in Figure 9. The approach used here is to apply sinusoidal frequency modulation to the input signal of radian frequency $\Omega$ and peak frequency deviation $\Delta\omega_s = 2\pi \Delta f_s$. Thus the PLL input signal is

$$v_{RF}(t) = A \sin \left[ 2\pi f_0 t + \frac{\Delta\omega_s}{\Omega} \sin(\Omega t) \right]$$

(6)

Under steady state conditions the loop error signal $\phi(t)$ is of the form

$$\phi(t) = m_x \sin(\Omega t + \phi_x)$$

(7)

where for a high gain ($K \gg \omega_n$) second order loop of the type used here ($N = 1$)

$$m_x \approx \frac{\Delta\omega_s}{\sqrt{(\omega_n^2 - \Omega^2)^2 + 4\zeta^2 \omega_n^2 \Omega^2}}$$

(8)

We also know that $m_x$ is maximized when $\Omega = \omega_n$ and the maximum value is given by

$$\max_{\Omega} m_x = \frac{\Delta\omega_s}{2\zeta \omega_n}$$

(9)
If we define $\Omega'$ and $\Omega''$ as the upper and lower 3 dB frequencies with respect to the maximum value of $m_x$, then it can be shown that

$$\omega_n^2 = \Omega'\Omega''$$

$$2\zeta\omega_n = \Omega' - \Omega''$$

Thus by experimentally determining $\Omega'$ and $\Omega'$ using a frequency counter and an AC voltmeter connected to the phase detector output, as shown in Figure 9, $\omega_n$ and $\zeta$ can be determined.

- Using the test set-up shown in Figure 9 experimentally determine $\omega_n$ and $\zeta$ of the PLL. Make sure that the peak phase error which occurs when $\Omega = \omega_n$, does not significantly violate the loop linearity assumptions (e.g., $\max m_x < \pi/6$). When making this measurement you will notice considerable phase jitter on the phase error signal. This is due to the phase noise of both the input signal function generator and the VCO function generator. The oscillator phase noise creates a source of error that can be seen as a noise voltage bias on the AC voltmeter. The double frequency term at 100 MHz is also present, but can be rejected on the scope display by selecting HF reject as the input filtering mode.

- Turning away from the hardware, construct a VisSim/Comm simulation of the above PLL in baseband form, it does not need to be complex baseband as the nonlinear baseband model will suffice. Using the design values from the hardware PLL just studied, verify the performance of the simulation in terms of hold-in range, pull-in range, and closed loop sinusoidal FM response as a means for experimentally determining (verifying) $\omega_n$ and $\zeta$.

4 Second Order PLL with Integrator/Lead Compensation Loop Filter

In this section of the experiment the PLL will be redesigned using a loop filter which consists of an integrator with phase lead compensation. The loop filter transfer function is given by

$$F(s) = \frac{1 + st_2}{st_1}$$

and the op-amp implementation of this filter is as shown in Figure 10. From a design standpoint the major difference between this filter and the lead lag filter is that the integrator in the loop filter makes the hold-in range theoretically infinite (i.e $|KF(0)| = \infty$). In practice the hold-in range is only limited by the tuning range of the VCO.

4.1 Laboratory Exercises

The loop filter components $R_1$, $R_2$, and $C$ must be determined such that the system requirements are satisfied. Designing for a specific natural frequency, $\omega_n$, and damping factor, $\zeta$, follows directly from the PLL linear model equations.

- Determine suitable component values for $R_1$, $R_2$, and $C$ for an RF power level of -10 dBm to achieve $\omega_n = 5 \times 10^4$ rad/s, and $\zeta = 1/\sqrt{2}$. What is $\Delta f_H$? Again it is suggested that you initially choose a convenient value for $C$. 
Modify the original lead lag loop filter circuit to reflect the new loop filter component values.

Close the loop by connecting the level shifter output to the VCO control signal input. Verify phase lock by observing the VCO output on the Agilent 4395A spectrum analyzer (or HP 4195A). A potential problem with this loop filter that you may notice is that before the loop locks or perhaps while it is trying to lock, the op-amp integrator output may drift off into saturation. In practice a sweeping circuit may be connected around the loop filter to prevent saturation from occurring. If this is causing problems with your circuit try placing $R_3$ temporarily back into the circuit, then as soon as the loop locks, carefully remove $R_3$. The loop should remain locked.

Experimentally verify the “infinite” hold-in range provided by this loop filter by slowing raising and lowering the frequency of the Agilent 33250A. Is the hold-in range really infinite?

Using the test set-up shown in Figure 9 experimentally determine $\omega_n$ and $\zeta$.

5 Further Investigations

If time permits you may wish to verify additional PLL characteristics. These include transient response, the effects of changing $\omega_n$ and $\zeta$, and additive noise and oscillator phase noise effects on phase jitter.

5.1 Transient Response

The easiest transient response to view with the current test configuration is the frequency step response. This can be obtained by setting the frequency modulation function generator to produce square waves. To observe the entire response the square wave frequency should be less than $10\omega_n/(2\pi)$. Placing the scope on the VCO control voltage is a good place to observe the transient
response due to a frequency step. The VCO control voltage, \( e(t) \), is proportional to the instantaneous VCO frequency with the additional of the offset. In terms of an isolated rising edge of the applied square wave frequency modulation,

\[
e(t) = v_{\text{offset}} + \frac{\Delta f_s}{K_v} \mathcal{L}^{-1}\left\{ \frac{1}{s} H(s) \right\}
\]

where the units of \( K_v \) is here assumed to be Hz/v. For the lead-lag loop filter we know that for \( \zeta < 1 \)

\[
\mathcal{L}^{-1}\left\{ \frac{1}{s} H(s) \right\} = \mathcal{L}^{-1}\left\{ \frac{1}{s} \cdot \frac{(2\zeta \omega_n - \omega_n^2/K)s + \omega_n^2}{s^2 + 2\omega_n s + \omega_n^2} \right\}, \quad \zeta < 1
\]

\[
= 1 - e^{\xi_{\text{cont}}} \left[ \cos(\omega_n t \sqrt{1 - \zeta^2}) - \frac{\zeta - \omega_n/K}{\sqrt{1 - \zeta^2}} \sin(\omega_n t \sqrt{1 - \zeta^2}) \right] u(t)
\]

and for \( K > \omega_n^2 \) we have the same result as for the integrator with lead correction filter,

\[
\mathcal{L}^{-1}\left\{ \frac{1}{s} H(s) \right\} = \mathcal{L}^{-1}\left\{ \frac{1}{s} \cdot \frac{2\omega_n s + \omega_n^2}{s^2 + 2\omega_n s + \omega_n^2} \right\}, \quad \zeta < 1
\]

\[
= 1 - e^{\xi_{\text{cont}}} \left[ \cos(\omega_n t \sqrt{1 - \zeta^2}) - \frac{\zeta}{\sqrt{1 - \zeta^2}} \sin(\omega_n t \sqrt{1 - \zeta^2}) \right] u(t)
\]

The expected step response less a DC offset at the VCO input for the second order loops implemented in this lab is shown in Figure 11 for various values of \( \zeta \).

### 5.2 Changing \( \omega_n \) and \( \zeta \)

Different values of \( \omega_n \) and \( \zeta \) can be considered in terms of the effect on transient response, and also the effect on phase jitter due to oscillator phase noise. Phase jitter is of particular interest here since the reference source, the Agilent 33250A function generator, is not particularly clean. To verify this you may wish to redesign one of the loop filters with \( \omega_n \) reduced by a factor of five or ten. Then try to lock the loop and observe changes in the of amount of phase jitter that is present. Increasing \( \omega_n \) above the original design point should have an opposite effect on phase jitter. With the present lowpass filter on the phase detector output \( \omega_n \) cannot be increased too much without running into stability problems due to spurious time constant effects.

### 5.3 Phase Noise Characterization

The spectrum analyzer can be used to measure the phase noise. To compare with theory, we can create a behavioral level model in Spice (XSpice) that will include phase noise from the input source, VCO, and the noise from the op-amp and the remaining electronic circuitry. Figure 12 shows a simulation model useful in modeling the phase noise in the PLL module. Attempting to match theory is another area for further investigation. More information on how to do this effectively may be available in the final release of this lab document.
Figure 11: Frequency step response, less a DC offset, as seen at the VCO input for a second order PLL with integrator/lead compensation loop filter.

Figure 12: Phase noise modeling.
# Appendix: Data Sheets

## 6.1 VCO

### Notes
- For Surface Mount Environmental Specifications, please click [here](#).
- Reflow soldering information is available in "Surface Mount" article.
- Non-hermetic.
- Operating Temperature: -65°C to +85°C
- Absolute Max. Supply Voltage ($V_{DD}$) +16V and Tuning Voltage ($V_{tune}$) +18V
- General Quality Control Procedures and Environmental Specifications are given in [Mini-Circuits Guar](#)
- Hi-Rel MIL description are given in [Hi-Rel and MIL](#).
- Prices and Specifications subject to change without notice.

### JTOS-75

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<th>Power Output dBr</th>
<th>Tuning Voltage V</th>
<th>Phase Noise dBc/Hz @ 1kHz offset frequencies: Typ.</th>
<th>Pulling Mhz pk-pk @ 12 dB</th>
<th>Pushing Mhz/ V</th>
<th>Tuning Sensitivity dBC @ 1kHz</th>
<th>3dB Modulation Bandwidth kHz</th>
<th>Power Supply mA Max.</th>
<th>Voltage V Min. Max.</th>
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* applies to dual output VCO.

### Pin Connections

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### Case Styles: BK377

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<td>D</td>
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Tolerance: ±1.00 ±0.03 ±0.015 inch.
6.2 Mixer (Phase Detector)

**Frequency Mixers**

**LO Power Level 4 dBm**

**Pin Configuration**

Port: LO RF IF Ground Grid Not Used

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<th>3</th>
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<td>N</td>
<td>M</td>
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</table>

**Outline Drawing**

**Frequency Specifications**

**ADEX-10L**

| Frequency MHz | LO Power Level 4 dBm | Conversion Loss (dB) | LO | LO | LO | LO | LO | LO | LO | LO |
|---------------|-----------------------|----------------------|----|----|----|----|----|----|----|----|----|
| LO RF IF      | Mid Band Total Range  |                     | U |    |    |    |    |    |    |    |    |
| 10.00 GHz     | 3.00 GHz              |                      |   |    |    |    |    |    |    |    |    |
|              | 0.50 GHz              |                      |   |    |    |    |    |    |    |    |    |

**Notes:**
- Absolute maximum power, voltage and current ratings:
  - RF power: 50mW
  - Peak IF current: 40mA
- 1 dB Conversion loss: +1 dBm typ.
- For Surface Mount Environmental Specifications, please click here.
- Conversion loss increases 0.6 dB when IF is above 100 MHz.
- General Quality Control Procedures and Environmental Specifications are given in Mini-Circuits Quality Standard MIL-R-9763. MIL description are given in MIL-R-9763 and MIL.
- Prices and Specifications subject to change without notice.

**Electrical Specifications**

**ADEX-10L**

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<th>Conversion Loss (dB)</th>
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<th>LO</th>
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<tr>
<td>LO RF IF</td>
<td>Mid Band Total Range</td>
<td></td>
<td>U</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.00 GHz</td>
<td>3.00 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.50 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Typical Performance Data**

**ADEX-10L**

<table>
<thead>
<tr>
<th>Frequency MHz</th>
<th>LO Power Level 4 dBm</th>
<th>Conversion Loss (dB)</th>
<th>LO</th>
<th>LO</th>
<th>LO</th>
<th>LO</th>
<th>LO</th>
<th>LO</th>
<th>LO</th>
<th>LO</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO RF IF</td>
<td>Mid Band Total Range</td>
<td></td>
<td>U</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.00 GHz</td>
<td>3.00 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.50 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.3 Power Splitter

Notes:
- Aqueous washable. For non-aqueous requirements, LRPS units available in case style QQQ130.
- For Surface Mount Environmental Specifications, please click [here](#).
- Re-flow soldering information is available in "Surface Mount" article.
- Internal load dissipation: 0.125 Watt.
- Matched power rating: 2 Watt.
- Non-hemetic.

General Quality Control Procedures and Environmental Specifications are given in [Mini-Circuits Guaranty](#), Hi-Rel, MIL description are given in [Hi-Rel and MIL](#).

Prices and Specifications subjects to change without notice.

### ADP-2-1W 2 Way-0°

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Isolation (dB)</th>
<th>Insertion Loss, dB Above 3.0d</th>
<th>Phase Unbalance Degrees</th>
<th>Amplitude Unbalance, dB</th>
<th>Power Input, W</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000 - 650</td>
<td>30</td>
<td>20</td>
<td>20</td>
<td>100</td>
<td>80</td>
</tr>
</tbody>
</table>

L=low range(fL to 10fL), M=mid range(10fL to fL/2), U=upper range(fL/2 to fL)

**Pin Connections**

<table>
<thead>
<tr>
<th>Port</th>
<th>Sum</th>
<th>Port</th>
<th>Port</th>
<th>Port</th>
<th>Grd</th>
<th>Ext</th>
<th>Not Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>4</td>
<td>6</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Case Style - CD936 (inch,mm)**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>J</th>
</tr>
</thead>
<tbody>
<tr>
<td>.200</td>
<td>.100</td>
<td>.220</td>
<td>.100</td>
<td>.162</td>
<td>.005</td>
<td>.100</td>
<td>.050</td>
<td></td>
</tr>
<tr>
<td>7.112</td>
<td>7.784</td>
<td>5.588</td>
<td>2.640</td>
<td>4.115</td>
<td>1.397</td>
<td>2.640</td>
<td>.762</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>K</th>
<th>L</th>
<th>M</th>
<th>N</th>
<th>P</th>
<th>Q</th>
<th>R</th>
<th>S</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>.000</td>
<td>.300</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.651</td>
<td>7.620</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Tolerance: ±.01 inch.
## Op-Amp


**JFET-INPUT OPERATIONAL AMPLIFIERS**

... = 1, RS ≤ 1 kΩ, RL ≥ 2 kΩ, 0.003%

---

### electrical characteristics, $V_{CC} = \pm 15$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS†</th>
<th>$T_A$</th>
<th>TL081M, TL082M</th>
<th>TL084Q, TL084M</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$</td>
<td>$VO = 0, RS = 50 \Omega$</td>
<td>25°C</td>
<td>3</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>$\alpha_{VO}$</td>
<td>$VO = 0, RS = 50 \Omega$</td>
<td>Full range</td>
<td>9</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>$I_O$</td>
<td>$VO = 0$</td>
<td>25°C</td>
<td>5</td>
<td>100</td>
<td>5</td>
</tr>
<tr>
<td>$I_B$</td>
<td>$VO = 0$</td>
<td>25°C</td>
<td>30</td>
<td>200</td>
<td>30</td>
</tr>
<tr>
<td>$V_{ICR}$</td>
<td>Common-mode input voltage range</td>
<td>25°C</td>
<td>±12</td>
<td>±12 to</td>
<td>±12 to</td>
</tr>
<tr>
<td>$V_{OM}$</td>
<td>Maximum peak output voltage swing</td>
<td>$RL = 10 , \Omega$</td>
<td>25°C</td>
<td>±12</td>
<td>±12</td>
</tr>
<tr>
<td>$A_{VD}$</td>
<td>Large-signal differential voltage amplification</td>
<td>$VO = 0, R_L \geq 2 , \Omega$</td>
<td>25°C</td>
<td>25</td>
<td>200</td>
</tr>
<tr>
<td>$B_1$</td>
<td>Unity-gain bandwidth</td>
<td>25°C</td>
<td>3</td>
<td>3</td>
<td>MHz</td>
</tr>
<tr>
<td>$I_{1}$</td>
<td>Input resistance</td>
<td>25°C</td>
<td>10$^{12}$</td>
<td>10$^{12}$</td>
<td>Ω</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common-mode rejection ratio</td>
<td>$V_{IC} = V_{ICRn}$, $V_{O} = 0, RS = 50 , \Omega$</td>
<td>25°C</td>
<td>80</td>
<td>86</td>
</tr>
<tr>
<td>$S_{SVR}$</td>
<td>Supply voltage rejection ratio</td>
<td>$V_{CC} = \pm 15$ V to ±9 V, $VO = 0, RS = 50 , \Omega$</td>
<td>25°C</td>
<td>80</td>
<td>86</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply current (per amplifier)</td>
<td>$VO = 0$, No load</td>
<td>25°C</td>
<td>1.4</td>
<td>2.8</td>
</tr>
<tr>
<td>$V_{O1/V_{O2}}$</td>
<td>Crosstalk attenuation</td>
<td>$AVD = 100$</td>
<td>25°C</td>
<td>120</td>
<td>120</td>
</tr>
</tbody>
</table>

*All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as is possible.

---

### operating characteristics, $V_{CC} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$SR$</td>
<td>$V_I = 10 , \Omega$, $RL = 2 , \Omega$, $CL = 100 , \mu F$, See Figure 1</td>
<td>$V_I = 10 , \Omega$, $RL = 2 , \Omega$, $CL = 100 , \mu F$, See Figure 1</td>
<td>8°</td>
<td>13</td>
<td>V/μs</td>
</tr>
<tr>
<td>$t_r$</td>
<td>$V_I = 20 , \mu V$, $RL = 2 , \Omega$, $CL = 100 , \mu F$, See Figure 1</td>
<td>See Figure 1</td>
<td>0.05</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>$t_{OS}$</td>
<td>$V_I = 10 , \Omega$, $RL = 2 , \Omega$, $CL = 100 , \mu F$, See Figure 1</td>
<td>$f = 1 , kHz$</td>
<td>18</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>$v_{in}$</td>
<td>$R_S = 20 , \Omega$</td>
<td>$f = 10 , Hz$ to 10 kHz</td>
<td>4</td>
<td>μV</td>
<td></td>
</tr>
<tr>
<td>$I_{in}$</td>
<td>$R_S = 20 , \Omega$, $f = 1 , kHz$</td>
<td>0.01</td>
<td>pA/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>$V_{rms} = 6 , \text{V}$, $f = 1 , kHz$, $AVD = 1$, $RL \leq 1 , \Omega$, $RL \geq 2 , \Omega$</td>
<td>$0.003%$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*On products compliant to MIL-PRF-38535, this parameter is not production tested.