Introduction

In this project MATLAB will be used to perform a discrete-time simulation of a direct-sequence spread-spectrum (DSSS) communication system in the presence of jamming. The intent of this project will be for the student to become more familiar with using MATLAB for Monte Carlo type simulation, and also to compare simple analytical models for jamming performance analysis with actual simulation results. One serious drawback when performing discrete-time of any DSSS system is that simulating system with high processing gain is impractical due to the large number of samples that must be processed by the simulation. For this project the ratio of chip rate, $R_c$, to bit rate, $R_b$, will be kept reasonable. The basic system block diagram is shown below in Figure 1. The minimum simulation requires at least one sample per chip. For chip level waveform fidelity,

$$R_b = 1$$

from say four to 16 samples per chip may be needed. In actual DSP hardware systems two or three

![Figure 1: General complex baseband BPSK DSSS system simulation block diagram with tone jamming.](image)
samples per chip is used.

The project is to be worked individually by each student. Do your own work. The due date for the completed project will be Monday, August 8, 2005.

Performance Analysis

Consider a single tone jammer of the form

\[ s_j[n] = \sqrt{P_j} \exp[2\pi \Delta f n + \theta] \]  

(1)

where \( P_j \) is the jammer power and in terms of the normalized digital frequency, \(-1/2 < \Delta f < 1/2\). Note that the effective system sampling rate in samples per second is

\[ F_s = N_c \times R_c = N_c \times R_b \times \frac{N_b}{N_c} = N_b \times R_b \mid R_b = 1 = N_b \]  

(2)

so the usable bandwidth for positioning the jammer with respect to the nominal carrier frequency (here at 0 Hz), is \(-N_b/2 < F_j < N_b/2\).

Bit Error Probability for a Single Tone Jammer

The results of [1] valid for a long spreading code period and \( R_c/R_b > 10 \) are easily calculated. The only catch is that the bit error probability is dependent on the relative phase, \( \theta \), between the jammer and the DSSS signal. For BPSK DSSS the conditional probability of bit error (conditional BEP) given an on-tune jammer, is

\[ P_e(z|\theta) = Q \left\{ \left[ \frac{N_0}{2E_b} + \frac{\text{JSR}}{N} \cos^2 \theta \right]^{-1/2} \right\} \]  

(3)

where \( z = E_b/N_0 \) is the ratio of the signal energy per bit to the noise power spectral density, JSR is the jammer-to-signal ratio, \( N = R_c/R_b \) is the system processing gain, and \( Q() \) is the Gaussian \( Q \)-function defined as

\[ Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\frac{u^2}{2}} du \]  

(4)

For the off-tune jammer at frequency \( \Delta F \) with respect to chip rate \( R_c \), the conditional BEP is

\[ P_e(z|\theta) = Q \left\{ \left[ \frac{N_0}{2E_b} + s_1^2 \frac{\text{JSR}}{2N} \left( 1 + \frac{s_2}{N} \cos \theta \right) \right]^{-1/2} \right\} \]  

(5)

where

\[ s_1 = \frac{2N}{2\pi \Delta F / R_b} \sin \left( \frac{2\pi \Delta F}{2R_c} \right) \]  

(6)

\[ \sin \left( \frac{2\pi \Delta F}{R_b} \right) \]  

\[ s_2 = \frac{\sin \left( \frac{2\pi \Delta F}{R_c} \right)}{\sin \left( \frac{2\pi \Delta F}{R_b} \right)} \]  

(7)
and the previous definitions still hold. Note that $\Delta F$ is the jamming frequency offset from the carrier in Hz.

The average BEP, assuming the tone jammer phase is uniform on $[0, 2\pi]$ is

$$P_e(z) = \frac{1}{2\pi} \int_{0}^{2\pi} P_e(z|\theta) f_\theta(\theta) \, d\theta = \frac{1}{2\pi} \int_{0}^{2\pi} P_e(z|\theta) \, d\theta$$

(8)

Evaluation of (8) will require numerical integration, e.g. MATLAB’s \texttt{quadl()} or similar. For the simulation to model the above phase distribution you must insure that the jammer is not synchronous with the chip rate.

**Specific Projects Tasks**

1. Obtain a reference plot of BEP versus $E_b/N_0$ without any jamming to verify proper noise calibration. Fix the spreading ratio at $N = 16$. It will be time consuming, but you will need to obtain at least 100 errors per BEP data point to have reasonable confidence about your $P_e$ values.

2. Plot theoretical BEP plots versus $E_b/N_0$ for various values of processing gain, $N$, jammer-to-signal ratio, JSR, and chip rate normalized jammer offset frequency, $\Delta F/R_c$. In particular consider combinations of JSR = −10, 0, 10, and 20 dB, $N = 16, 32, 64, 128$, and $\Delta F/R_c = 0, 0.5, 1.5$. What happens when $\Delta F/R_c$ is an integer other than zero?

3. Repeat a few of the curves obtained in part 2 via simulation. How do your results compare? How sensitive is the simulation to near synchronous jammer frequencies?

**References**