RF Receiver
Hardware Design

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Topics

• Customer Requirements
• Communication link environment
• Performance Parameters/Metrics
• Frequency Conversion Architectures
• I/Q Demodulation Architectures
• Example Design Based on a Real Product
• Receiver RF Modeling
• My career history
Customer Requirements

• Who was my customer?
  – My employer
  – Various groups with similar but slightly different applications

• Requirements
  – 70 MHz input center frequency
  – Industry standard cPCI form factor
  – Detailed RF requirements coming up

• Internally generated requirements are often vague

• Ill-defined requirements can easily lead to schedule slips and cost over-runs
• Wireless (RF) link between transmitter and receiver
• Input signal to receiver may vary in amplitude
• Interference may be present
• RF spectrum is crowded (adjacent channel interference)
• Desire low Bit Error Rate (BER) at high data rates
• Design goal: Optimize receiver performance under variable conditions (in this presentation under variable signal amplitude only)
• Receiver Performance Dependent on Signal Strength

• Small signal performance generally dictated by AWGN (w/o fading)
  – Noise Bandwidth
  – Noise Figure
  – Signal-to-Noise ratio (SNR), Signal-to-Noise Density ratio (S/No)
  – Eb/No

• Large signal performance generally dictated by receiver linearity
  – Intermodulation Distortion
    • Spectral spreading, re-growth, etc
    • 3rd Order Intercept Point
  – Harmonic Distortion
  – Amplitude Compression

• Receiver design can be optimized for
  – Small signal performance
  – Large signal performance
  – A combination/balance of small and large signal performance
Frequency Conversion Architectures

Super heterodyne

1st LO frequency = RF - IF (or RF + IF)

2nd LO frequency = IF frequency

Direct Conversion

LO frequency = RF frequency
Frequency Conversion Trade-offs

• Super heterodyne
  – High performance, high cost
  – Distributed frequency plan allows distributed filtering and gain

• Direct Conversion Benefits
  – Fewer parts
    • Image reject filter
    • IF bandpass filter
    • 1\textsuperscript{st} Local Oscillator
  – Smaller and lower cost

• Direct Conversion Issues
  – DC offsets
  – LO leakage
  – 2\textsuperscript{nd} order distortion
  – 1/f noise (flicker noise)
Direct Conversion Issues

• DC Offsets in baseband I/Q signals
  – Caused by LO self-mixing and baseband circuitry
  – Offset amplitude varies with RF frequency and antenna effects
  – Mitigated by compensation/calibration, near-zero IF, AC coupling, etc

• LO Leakage Out of Receiver
  – LO is at RF frequency and cannot be filtered
  – Leakage amplitude dependent upon isolation of components

• 2\textsuperscript{nd} Order Distortion with two input signals at frequencies $f_1$ and $f_2$
  – 2\textsuperscript{nd} order distortion is at $|f_1-f_2|$ and $f_1+f_2$
  – $|f_1 - f_2|$ problematic when $f_1$ and $f_2$ are in-band and close in frequency
  • Distortion is near DC and interferes with desired I/Q baseband signals

• 1/f Noise (flicker noise) is intrinsic in semiconductor devices
  – Coupling of 1/f noise with desired signal is predominately at baseband
  – Direct conversion has smaller signals (and more gain) at baseband
  – SNR degradation is more pronounced as compared with super heterodyne
I/Q Demodulation Architectures

Analog I/Q Demodulation

Digital (DSP) I/Q Demodulation
I/Q Demodulation Trade-offs

• Digital I/Q Demodulation
  – I/Q gains are exactly equal and phase is exactly quadrature
  – Requires A/D sample rate at least 2x modulation bandwidth

• Analog I/Q Demodulation
  – I/Q gain and phase are not perfectly balanced
  – Imbalances create distortion
  – Requires A/D sample rate at least 1x modulation bandwidth

• For a given A/D converter capability, analog I/Q demodulation provides twice the modulation bandwidth at the expense of more hardware and higher distortion
IF Receiver Example: Requirements

- Input frequency is 70 MHz
- Modulation bandwidth up to 40 MHz (various data rates & modulation)
- Input signal amplitude -75 dBm to 0 dBm
- Input noise floor -150 dBm/Hz to -135 dBm/Hz (Not just thermal noise)
- Intermodulation distortion
  - -60 dBc for signal inputs up to -10 dBm
  - -50 dBc for signal inputs from -10 dBm to 0 dBm
Commercial A/D Converter technology provides 12 bits at 210 Msps
- Meets Nyquist criteria of greater than 2x the modulation BW (80 MHz)
- Digital I/Q demodulation architecture avoids imbalance distortion issues
- Over-sampling provides at least 5 samples per bit for high performance data demodulation and bit synchronization

75 dB of signal amplitude variation requires analog gain control

Gain required for adequate signal amplitude into A/D converter

Consider input noise floor
- 40 MHz noise bandwidth => 76 dB-Hz
- Input noise density of -135 dBm/Hz is -59 dBm (over 40 MHz)
- Receiver automatic gain control (AGC) operates on S+N
- Input SNR can be negative
IF Receiver Example: Critical Trade-offs

- Receiver must provide the necessary gain to bring the input signal to the optimum level into the A/D converter

- Too little gain => inadequate signal level into A/D
  - Instantaneous dynamic range limited by A/D quantization noise floor

- Too much gain => excessive signal level into A/D
  - With low SNRs, the A/D can saturate on noise “spikes”
  - Increased intermodulation distortion

- Optimum level into A/D dependent upon SNR, noise statistics, signal characteristics, and number of bits in the A/D
  - For small SNRs, Gaussian noise, sinewave input, and 12 bit A/Ds, the optimum amplitude into the A/D is about 14 dB below A/D fullscale*

IF Receiver Example: Design Approach

- IF Receiver product for a multitude of satellite communication applications
- Generic architecture consists of filters, amplifiers, variable attenuators, etc

![IF Receiver Diagram]

- Model the cascade of receiver components to predict performance
- Follow signal, noise, and distortion levels through each component in the receiver chain
- Calculate receiver performance metrics such as noise figure and input intercept point
• Noise Figure describes the SNR degradation caused by noise generated internally within the receiver

• Cascaded Noise Figure
  \[ NF_{\text{total}} = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{(G_1 \times G_2)} + \ldots \]

• In this example design, the system noise performance is dictated by external noise floor over most of the input signal amplitude range

• Third Order Intercept Point quantifies the intermodulation distortion created within the receiver

• Cascaded Third Order Input Intercept Point
  \[ IIP3_{\text{total}} = \frac{1}{\left\{ \frac{1}{IP3_1} + \frac{G_1}{IP3_2} + \frac{(G_1 \times G_2)}{IP3_3} \right\}} + \ldots \]
### IF Receiver Example: Cascaded Model

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<th>Component</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>Power Point</th>
<th>ICP</th>
<th>3rd Order</th>
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<th>NF (dB)</th>
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<th>ICP</th>
<th>3rd Order</th>
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**ADFS:** 1.536 V assumed to be pk-pk
**14 dB backoff:** 0.199526 linear
**Cascaded NF:** 13.54 dB set point: 0.306472 V assumed to be pk-pk

**Output power:** -15.80 dBm

**ADC input load impedance:** 200.0 ohms
**S+N:** -11.84 dBm
1st stage NF: 13.4 dB
2nd stage NF: 5.50 dB

**I/Q voltage:** 0.073 Vrms
**S+N voltage:** 0.114 Vrms
1st stage NF: 21.9 linear
1st stage gain: 5.70 dB
2nd stage NF: 3.55 linear
2nd stage contribution: 6.86E-01 linear

**Output SNR:** -1.7 dB
1st stage gain: 3.72 linear

**Total gain:** 59.2 dB

**Total SFDR:** 74.6 dB based only on 3rd order distortion
cascaded: 2.257E+01 linear 3rd stage NF: 10.50 dB
IF Receiver Example: Modeled Eb/No Performance

Output Eb/No vs. Input Signal Power
(input noise floor is -150 dBm/Hz)

-90 -80 -70 -60 -50 -40 -30 -20 -10 0

0 10 20 30 40 50 60 70 80

Eb/No (dB)

Input Power (dBm)

100 kbps 2 Mbps 10 Mbps 35 Mbps
$IF$ Receiver Example: Modeled Eb/No Performance (con't)

Output Eb/No vs. Input Signal Power
(input noise floor is -135 dBm/Hz)
IF Receiver Example: Modeled 3rd Order Intermodulation Distortion Performance

![3rd Order IMD vs. Input Signal Power Graph]
**IF Receiver Example: Modeled Noise Figure Performance**

**Noise Figure vs. Input Signal Power**

- Noise figure vs. input signal power graph with noise floors at -135 dBm/Hz and -150 dBm/Hz.
IF Receiver Example: Modeled SNR Degradation Performance

Noise floor = -135 dBm/Hz
Noise floor = -150 dBm/Hz
Questions
My Engineering Career

• BSEE 1983 from Iowa State University
  – Analog and communications focus

• 1982 to 1989: Hughes Aircraft Company, Los Angeles
  – Radar systems engineer primarily for RF and IF receivers

• 1989 to 1990: Research & Development Laboratories, Los Angeles
  – Radar and RF engineer for receiver design

• 1990 to 1994: NAVSYS, Monument, CO
  – GPS and RF engineer, project management, engineering management

• 1994 to 1996: XEL Communications, Aurora, CO
  – CATV data modem design

• 1996 to 2001: Mission Research Corporation, Colorado Springs
  – Fading channel emulators, military communications and radar systems, mgmt

• 2001 to 2003: Xircom/Intel, Colorado Springs
  – Commercial wireless modems, mgmt

• 2003 to present: RT Logic, Colorado Springs
  – Satellite communications, RF data links, radar, mgmt

MSEE from UCCS
1991-1996

MBA classes from UCCS
2009-present
Career Dialog

• What’s it like to be an engineer?

• Do I really need to remember all that calculus stuff?

• What career paths are available?

• What’s important and what’s not?
  – Salary
  – Challenge
  – Title
  – Writing
  – Math
  – Speaking
  – Company culture
  – Co-workers
  – Type of work

• In hindsight, would I do anything different?

• What if I don’t like engineering once I start working?

• How do I get, and hold, an engineering job?